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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/320,421	05/26/1999	LEONARD FORBES	303.586US1	4705

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/320,421	FORBES ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10,11,13-18,20-24,26-38 and 40-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10,11,13-18,20-24,26-38 and 40-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/30/2002 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 10, 11, 13, 14, 16-18, 20-24, 26, 27, 29-38, 44 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Austin (USP 5982690) in view of Chung (USP 5442209).

As to claim 10, Austin shows in figure 1D a latch circuit (105) comprising: a pair of cross-coupled amplifiers (153, 155 and 154, 156), wherein each amplifier includes: a transistor of a first conductivity type (155, 156); a pair field effect transistors (MOSFETs) of a second conductivity type (153, 154), wherein the drain region of the pair MOSFETs is coupled to a drain region of the transistor of the first conductivity type in the same amplifier, is coupled directly to a gate of the first transistor of the first conductivity type in the other amplifier of the pair of cross-couple amplifiers, and is coupled to a gate of the pair MOSFETs in the other amplifier of

the pair of cross-couple amplifiers; a pair of input transmission lines (outputs of circuit 103), wherein each one of the pair of input transmission lines is coupled to another gate of one of the pair MOSFETs in each amplifier, the pair of input transmission lines directly coupling the another gate in each amplifier external to the latch circuit; and a pair of output transmission lines (lat, /lat), wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the pair MOSFET. Thus, figure 1D shows all limitations of the claim except for the pair MOSFETs is a dual gated MOSFET. However, Chung teaches in figure 1 a MOS transistor comprising a single drain, a single source and plurality gates. This MOSFET having a function as plurality of transistors connected in parallel. The advantage of Chung's MOSFET is the chip area can be reduced in device fabrication. Therefore, it would have been obvious to one having ordinary skill in the art to make Austin's pair MOSFET (153 and 154) as a transistor having single drain, single source, and two gates (dual gated MOSFET) for the purpose of saving space.

As to claim 11, figure 1D shows the transistor of a first conductivity type is a p-channel metal oxide semiconductor (PMOS) transistor, and the dual-gated MOSFET include n-channel metal oxide semiconductor (NMOS) transistors.

As to claim 13, figure 1D shows the pair of input transmission lines are bit lines and the bit line capacitance are removed from the pair of output transmission lines.

As to claim 14, figure 1B shows circuit 51 coupled to memory array circuit. It is inherent that the memory array circuit comprising number of memory cells.

As to claim 16, Austin 's figure 1D shows all elements of the claims except for the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns). However,

it is well known in the art that the speed for the amplifier circuit dependent on the size of the transistors in the amplifier. Furthermore, Austin amplifier circuit having similar structure as Applicant amplifier circuit figure 2A. Therefore, Austin circuit is able to provide a full output of the sense voltage less than 10 nanoseconds depend on the size of the transistors in the amplifier. it is would have been obvious to one having ordinary skill in the art to modify the size of Austin amplifier circuit in order for the circuit is able to providing an output less than 10 nanoseconds because it is seen as a design choice.

As to claim 32, Austin's figures 1D, 4 and 5 and Chung's figure 1 show all elements of the claim except for the processor and memory are formed on the same semiconductor substrate and integrated circuit. However, it is well known in the art that elements that from on the same semiconductor substrate and integrated circuit having the advantage of matching temperature and space and cost saving. Therefore, it would have been obvious to one having ordinary skill in the art to make the processor and the memory to be formed on the same substrate and integrated circuit for the purpose of matching temperature and space or cost saving.

Claims 17, 18, 20-23, 26, 27, 29-31, 33-38, 44 and 45 recite similar limitations of claims 10, 11, 13-16. Therefore, they are rejected for the same reasons. Further called for claim 29, it is inherent for the memory circuit comprising a processor (figure 4).

As to claim 24, Austin's figure 1D shows the memory circuit includes a folded bit line memory circuit.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Austin (USP 5982690) in view of Chung (USP 5442209) and Ang et al (USP 5942918) (newly cited).

As to claim 15, the combination of Austin's figure 1D and Chung's figure 1 shows all elements of the claims except for the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts. However, Ang et al.'s figure 2 shows an amplifier circuit (231-233, 235, 237, 244-247) having similar structure with Austin amplifier circuit (105). Ang et al.'s amplifier circuit operable with a supply voltage less than 1 volts (column 1, lines 50-55). Furthermore, it is well known in the art that the power consumption of the circuit will be saved if it operates with a lower supply voltage. Therefore, it would have been obvious to one having ordinary skill in the art to select to supply Austin amplifier circuit with a voltage less than 1 volts for the purpose of saving power consumption.

5. Claims 28 and 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (U.S. Patent No. 6069828) in view of Austin (U.S. Patent No. 5982690) and Chung (USP 5442209).

As to claims 28 and 40, Kaneko et al. teaches in figure 2 a memory circuit, and a method thereof, comprising a number of memory arrays (two sides of sense amplifier 15); a sense amplifier (15), a complementary pair of bit lines (BL1, BL1, BL2, BL2) input to the sense amplifier, a number of equilibration (14a, 14b), and a number of isolation transistorsm(18a, 18b). Thus, figure 2 shows all elements of the claim except for the detail of the sense amplifier. However, Austin's figure 1D and Chung's figure 1 show a sense amplifier circuit (see the rejection above) comprising a pair of cross-coupled inverters (153, 155 and 154, 156), wherein each inverter includes: a PMOS transistor (155, 156), a dual-gated NMOS transistor (153, 154) wherein the drain region for the dual-gated NMOS transistor is coupled to a drain region of the PMOS transistor; a pair of bit lines (outputs of 103), wherein each one of the pair of bit lines is

coupled to a first gate of the dual-gated transistor in each inverter; and a pair of output transmission lines (out, /out), wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gated NMOS transistor and the drain region of the PMOS transistor in each inverter. Austin's amplifier circuit having the advantage of reducing power dissipation. Therefore, it would have been obvious to one having an ordinary skill in the art to use the Austin's sense amplifier circuit for Kaneko et al.'s figure 2 for the purpose of reducing power dissipation.

As to claim 41, Austin's figure 1D shows all elements of the claims except for the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts. However, the selection of the power supply to be less than 1.0 Volts is seen as an obvious design expedient dependent upon particular environment of use to ensure optimum performance.

As to claim 42, Austin 's figure 1D shows all elements of the claims except for the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns). However, it is also seen as a design choice for designing the output speed of the sense amplifier to be able to output a full output sense voltage in less than 10 nanoseconds (ns) dependent upon particular environment of use to ensure optimum performance.

As to claim 43, from the rejection above, it is inherent for the sense amplifier removes the bit line capacitance from a pair of output nodes of the sense amplifier.

Response to Arguments

Applicant's arguments have been fully considered but they are not persuasive. In response to the arguments in page 9, lines 2-11, figure 1D clearly shows the outputs of 103 are external connections to the latch circuit 105.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is (703) 308-6174. The examiner can normally be reached on Monday to Friday from 7:40 am to 4:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reach at (703) 308-4876. The fax phone number for this group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

QT

November 5, 2002

Terry D. Cunningham
Primary Examiner